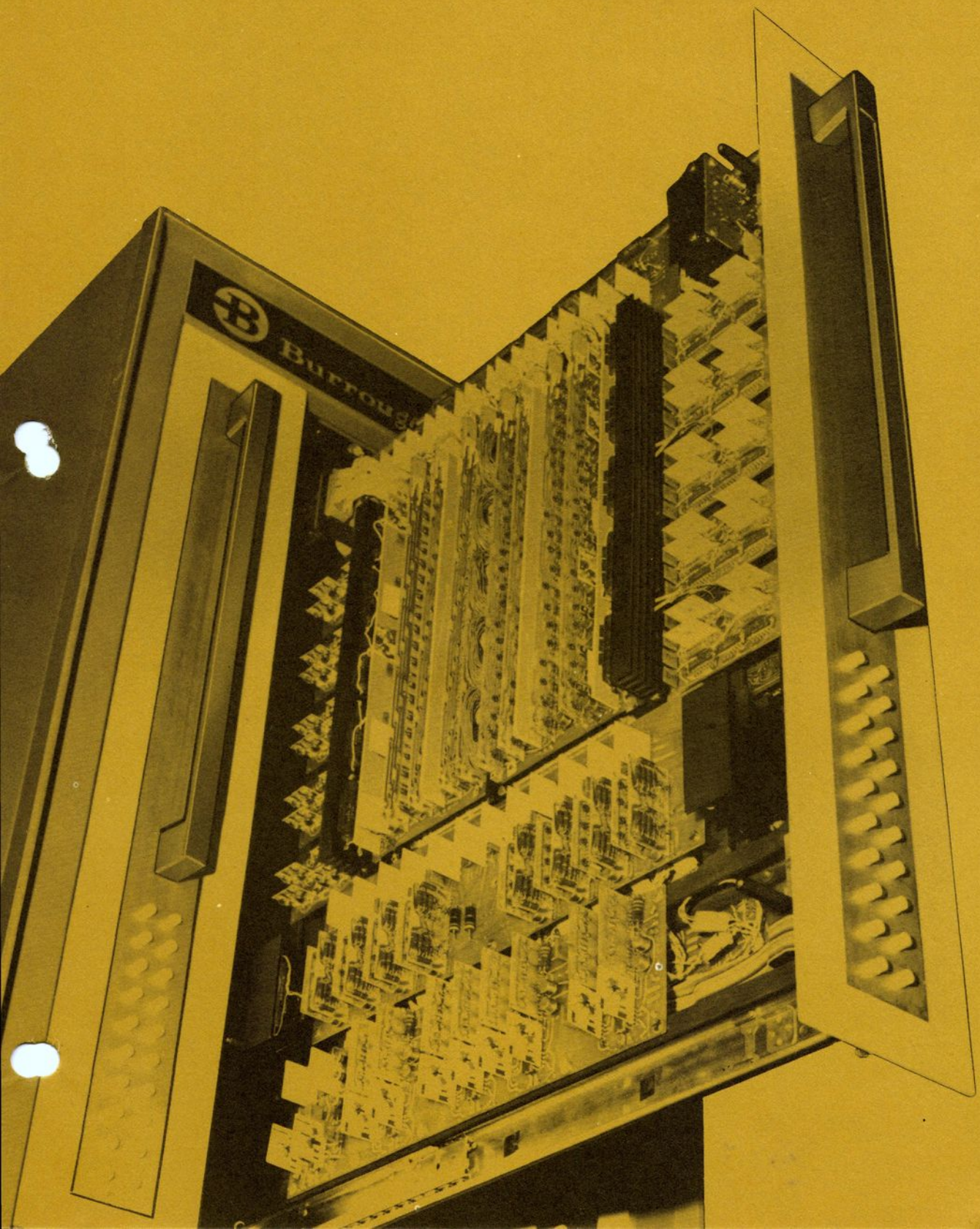
CORE MEMORY SYSTEMS



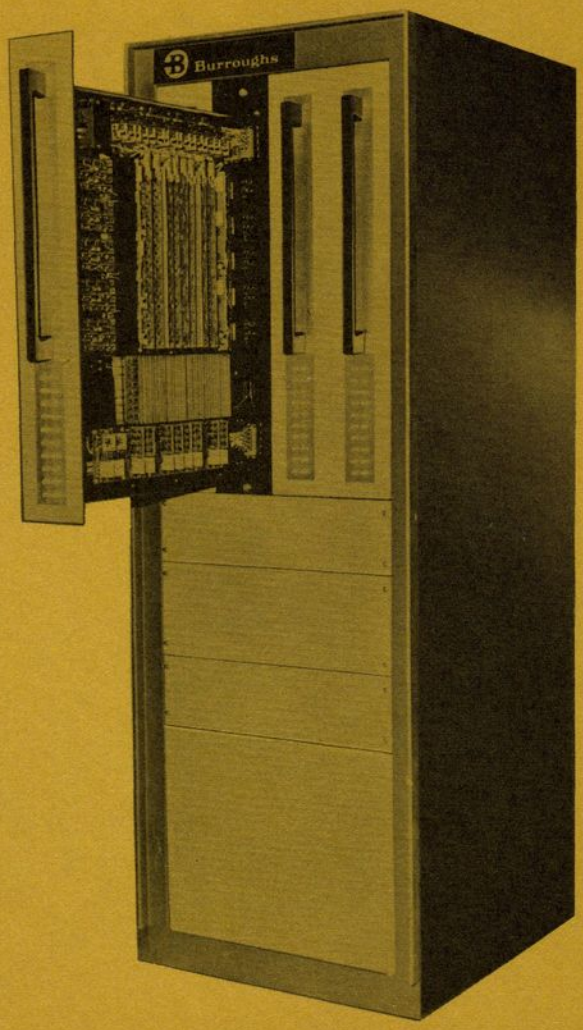
- **0.6 μsec. to 1.0 μsec. Cycle Times**
- **2½ D Organization**
- **20 mil cores**
- **Hybrid Microcircuits**
- **Monolithic Integrated Circuits**
- **Low Cost Per Bit**
- **Building-block Construction**
- **Standard Packaging**

The Burroughs BFC600 line of Core Memory Systems are random access, high speed systems for commercial, industrial and military data handling equipment. By using 20 mil cores (.020″ OD/.012″ ID) and a 2½ D wiring organization, full cycle times of 0.6 μsec is economically achieved. Reliability is enhanced by the use of Burroughs hybrid microcircuits in the line drivers and sense amplifiers. Monolithic integrated circuits are used for all logic and in the address and information registers.

The basic modular building block in the memory is 8192 words by 20 bits. Up to 4 of these modules which includes the core memory, sense amplifiers, driver circuits, and information registers can be accommodated vertically in a standard 19″ rack by 26¾″ panel height including mounting slides.

An associated memory control module which includes the timing circuits, address register and decode logic is also included. One control module is capable of servicing up to four memory modules and can be packaged in one of two mechanical configurations; one mounts horizontally in the standard 19″ rack. The other has identical dimensions of the basic memory module and may be mounted vertically, adjacent to the memory module(s). The latter may be employed when less than 4 memory modules are used.

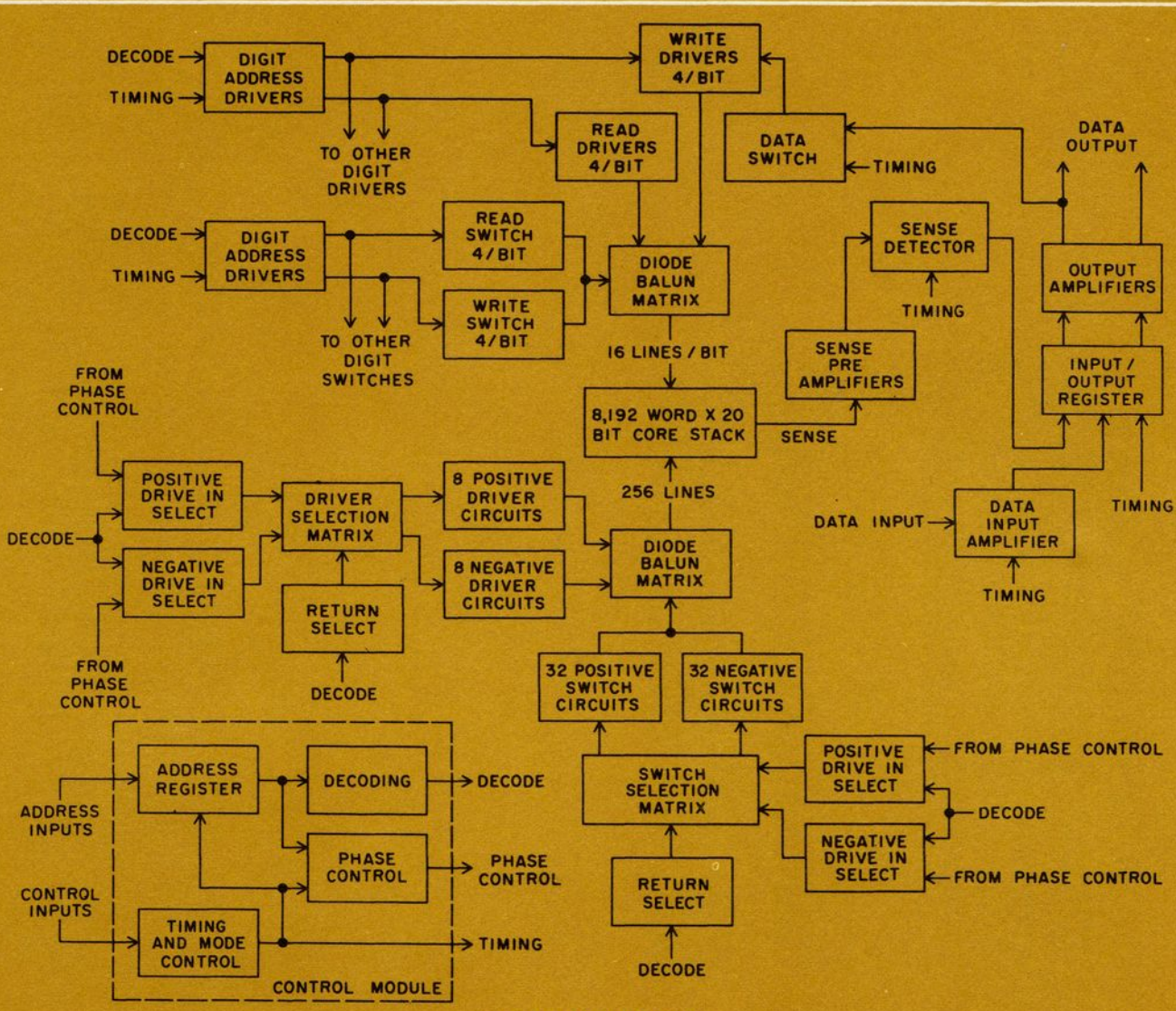
Power supplies capable of driving 4 memory modules and one control module are also available for 19″ rack mounting.



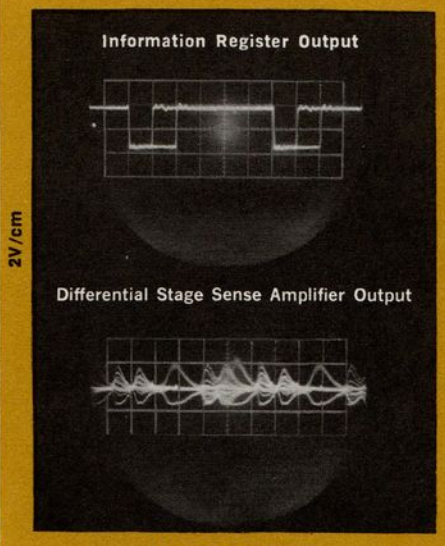
Console showing one memory module

SPECIFICATIONS

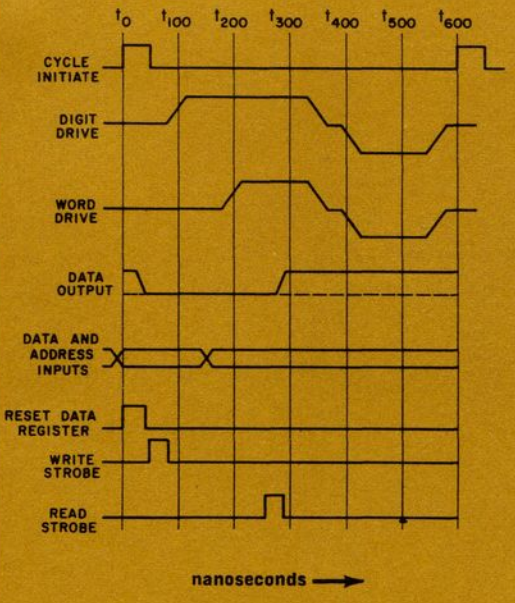
Memory Capacity	The modular construction lends the memory to a wide range of applications. Each building block can accommodate up to 8192 words of 20 bits per word. The module can easily be combined to build up both word capacity and bit length in any combination.
Mode of Access	Random, full cycle
Full Cycle Time	600 nanosecond to 1 microsecond
Access Time	Less than half the cycle time
Input Interface	All inputs accept twisted pair or coax cable with provisions for termination within the memory module
Standard Input Levels	Logic "1" = +2.2 ± 0.5V Logic "0" = −0.5 ± 0.5V
Power Dissipation	Less than 300 Watts per 20 bit module (worst case-all "1" condition).
Environmental Specifications	Temperature Range +15°C to +40°C Relative Humidity to 90% without condensation
Package Size (8192 word x 20 bit)	The memory module is 26¾″ high (including mounting slides), by 20½″ in depth (including mating connectors) by 4¼″ wide. The modules are front access, slide mounted units. Four of these modules will mount in a standard 19″ rack
Output Interface	Output data lines are driven by monolithic integrated buffer circuits that are capable of driving twisted pair or coax cable terminated in their characteristic impedance (not to be lower than 50 ohms).
Standard Output Levels	Logic "1" = +2.3 ± 0.4V Logic "0" = −0.5 ± 0.5V



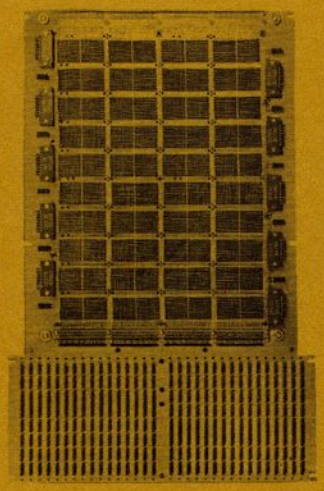
System block diagram



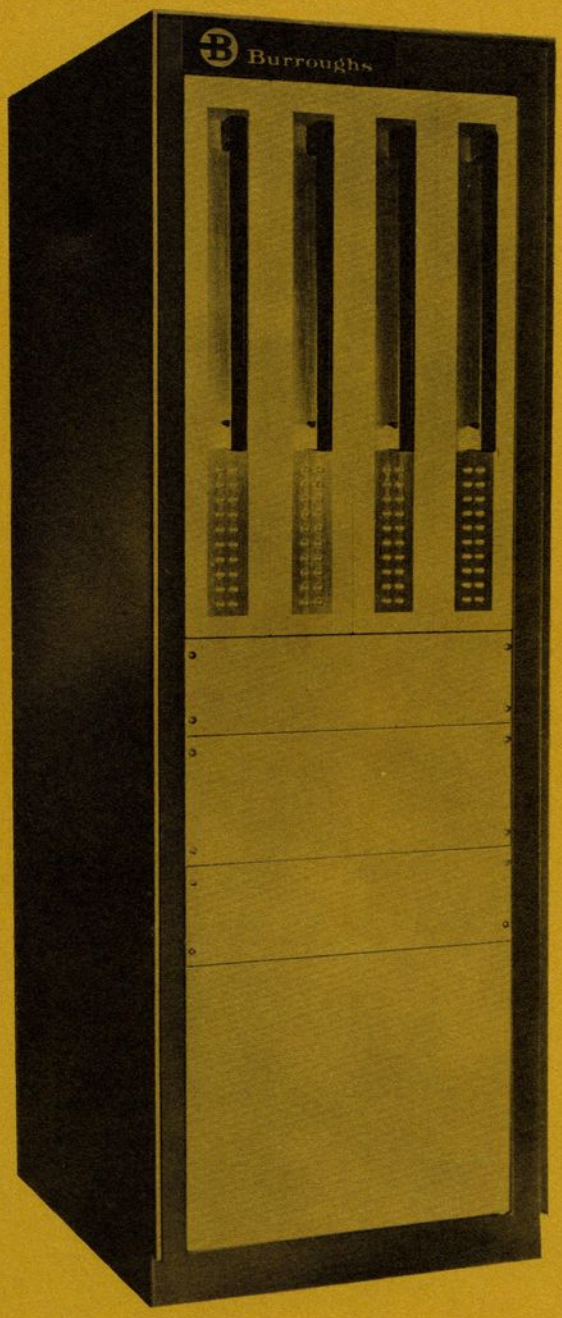
100 nanosec/cm



System Timing Diagram



2½ D Core memory Stack



Console containing memory modules, control module and power supplies.

ADDITIONAL FEATURES

Pluggable core stack
Selection diodes are mounted on pluggable boards
Low power consumption
All silicon semiconductors
Monolithic integrated logic circuits
Delay line timing
Data and address indicators
Easy access to all cores & memory lines

STANDARD OPTIONS AVAILABLE

Split cycle operation
Data retention
Special timing pulses
Margin control
Over-under voltage sensing
Built in self-test
Double rail data output
Special interface levels
Parity check and generation
Sequential access mode
250 nanosecond access time

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